UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte RICHARD SLOBODNIK, STEPHEN JOHN HILL,
and GERARD RICHARD WILLIAMS

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Appeal 2007-0576
Application 10/025,816
Technology Center 2100

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Decided: March 20, 2007

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Before JOSEPH F. RUGGIERO, LANCE LEONARD BARRY, and
HOWARD B. BLANKENSHIP, *Administrative Patent Judges*.

BARRY, *Administrative Patent Judge*.

I. STATEMENT OF THE CASE

A Patent Examiner rejected claims 1-34. The Appellants appeal therefrom under 35 U.S.C. § 134(a). We have jurisdiction under 35 U.S.C. § 6(b).

A. INVENTION

The invention at issue on appeal concerns self-testing of memories. Memories sometimes feature built-in self-test ("BIST") mechanisms for conducting self-tests to detect any memory defects. Because defects may vary from design to design and may vary with different fabrication processes applied to the same design, explain the Appellants, self-test methodologies are selected and tuned to a particular design and fabrication technique by the concerned manufacturer. A manufacturer will typically have a preferred test methodology that experience has taught is well suited to its particular environment. The test methodology adopted by one manufacturer, however, may not work for another manufacturer. (Specification 2.)

By varying address sequencing, in contrast, the Appellants' programmable self-test controller allows different test methodologies to be performed. (*Id.* 3.) Their self-test controller can handle the different test requirements of different manufacturers or the different test requirements that may arise for a single manufacturer as it develops its fabrication processes. (*Id.* 3-4.)

Claim 1, which further illustrates the invention, follows:

1. Apparatus for processing data, said apparatus comprising:

at least one memory having a plurality of memory storage locations associated with respective memory addresses; and

a self-test controller operable to control self-test of said at least one memory; wherein

said self-test controller is responsive to a self-test
instruction specifying a test methodology to be applied to
perform at least one memory access to each memory location
within a sequence of memory storage locations, memory
address changes between successive memory locations accessed
within said sequence of memory storage locations being
selected in dependence upon said self-test instruction such that
said self-test controller may be configured by said self-test
instruction to implement different memory test methodologies.

B. REJECTIONS

Claims 1-9, 13, 16-26, 30, 33, and 34 stand rejected under 35 U.S.C. §
102(b) as anticipated by U.S. Patent No. 5,661,732 ("Lo"). Claims 10, 11,
14, 27, 28, and 31 stand rejected under 35 U.S.C. § 103(a) as obvious over
Lo and U.S. Patent Application Pub. No. 2003/0167428 ("Gold").
Claims 12, 15, 29, and 32 stand rejected under § 103(a) as obvious over Lo
and U.S. Patent No. 6,001,662 ("Correale").

III. PROCEDURAL MATTER

The Evidence Appendix of an Appeal Brief shall "contain[ ] copies of
any evidence submitted pursuant to §§ 1.130, 1.131, or 1.132 of this title or
of any other evidence entered by the examiner and relied upon by appellant
in the appeal, along with a statement setting forth where in the record that
evidence was entered in the record by the examiner." 37 C.F.R.
§ 41.37(c)(1)(ix) (2005).[1] Here, although the Appellants rely on the
"definition of methodology . . . contained in Webster's 9th New Collegiate

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[1] We cite to the version of the Code of Federal Regulations in effect at the
time of the Appeal Brief.

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Dictionary," (Pre-Appeal Brief Request for Review 1), their Evidence Appendix omits the definition, instead indicating "None." (Br. A12.) The Appellants should provide a copy of the definition in their next communication with the United States Patent and Trademark Office.

III. ISSUE

Rather than reiterate the positions of the Examiner or the Appellants *in toto*, we focus on the issue therebetween. The Examiner makes the following assertion.

> Lo teaches the claimed "a self-test instruction specifying a test methodology". For example, if one skilled in the art using Lo's ABIST engine 12 received a single 9-bit word (**a self-test instruction**) from the Microcode Array 10 containing a "010" in the Micro-code Array Address Pointer field 14, a "1" in the Address Increment field 15, "000" in the Data Pattern Control field 16, a "1" in the Read/Write Control Field 17, and a "1" in the End-of -Address-Space Control field 18 from the Microcode Array 10, that is 0101000111 [sic], a test methodology (i.e. a body of methods, rules, and postulates employed by a discipline: a particular procedure or set of procedures) would be executed to set the ABIST engine 12 in write mode (Read/ Write Control Field 17, Col. 11, Table 8), increment the memory address (Address Increment field 15, Col. 10, Table 6), Shift and Rotate (Data Pattern Control field 16, Col. 10, Table 7), detect the end of address (End-of - Address-Space Control field 18, Col. 11, Table 9) and do all this repeatedly (hold the ROM pointer) until the address space has been fully explored at which time the ROM pointer is incremented to one (Micro-Code Array Address Pointer field 14, Table 5, Col. 8). These "set of procedures" (**specifying a test methodology**) are executed as a result of **one single** 9-bit word (**a self-test instruction**) read from the microcode

array 10, not from eight different 9-bit words as the appellants
contend. . . .

(Answer 12-13.) The Appellants argue, "Table 8 is a clear admission that
each single 9-bit word can only either Read or Write and cannot do both."
(Reply Br. 3.) Therefore, the issue is whether Lo teaches a single instruction
specifying a sequence of testing procedures.

"In addressing the point of contention, the Board conducts a two-step
analysis. First, we construe independent claims at issue to determine their
scope. Second, we determine whether the construed claims are anticipated
or would have been obvious." *Ex Parte Tomlinson*, No. 2005-0100,
2005 WL 4773715, at *2 (B.P.A.I. 2005).

IV. CLAIM CONSTRUCTION

Our analysis begins by interpreting the claim limitations at issue.
"[W]hen interpreting a claim, words of the claim are generally given their
ordinary and accustomed meaning, unless it appears from the specification
or the file history that they were used differently by the inventor." *In re
Paulsen*, 30 F.3d 1475, 1480, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994)
(citing *Carroll Touch, Inc. v. Electro Mechanical Sys., Inc.*, 15 F.3d 1573,
1577, 27 USPQ2d 1836, 1840 (Fed. Cir. 1993)).

Here, claim 1 recites in pertinent part the following limitations:
"a self-test instruction specifying a test methodology. . . ." Claim 18 recites
similar limitations. It is uncontested that the ordinary and accustomed
meaning of methodology "is 'a body of methods, rules, and postulates

employed by a discipline: a particular procedure or set of procedures.'" (Br.
9.) Giving the limitations their ordinary and accustomed meaning, therefore,
the two independent claims require a single instruction that specifies a
sequence of testing procedures.

V. ANTICIPATION AND OBVIOUSNESS DETERMINATION

"Having construed the claim limitations at issue, we now compare the
claims to the prior art to determine if the prior art anticipates those claims."
In re Cruciferous Sprout Litig., 301 F.3d 1343, 1349, 64 USPQ2d 1202,
1206 (Fed. Cir. 2002). "A claim is anticipated only if each and every
element as set forth in the claim is found, either expressly or inherently
described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union
Oil Co.*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (citing
Structural Rubber Prods. Co. v. Park Rubber Co., 749 F.2d 707, 715, 223
USPQ 1264, 1270 (Fed. Cir. 1984); *Connell v. Sears, Roebuck & Co.*, 722
F.2d 1542, 1548, 220 USPQ 193, 198 (Fed. Cir. 1983); *Kalman v. Kimberly-
Clark Corp.*, 713 F.2d 760, 771, 218 USPQ 781, 789 (Fed. Cir. 1983)).
"[A]bsence from the reference of any claimed element negates anticipation."
Kloster Speedsteel AB v. Crucible, Inc., 793 F.2d 1565, 1571, 230 USPQ 81,
84 (Fed. Cir. 1986).

Here, Lo "us[es] a built in array test system that is programmable in
computer systems to enable testing of chip arrays whose address space has
two different logical views." (Col. 1, ll. 29-31.) More specifically, the
reference's "ABIST engine 12 receives a 9 bit word 13 from a Microcode
Array 10 which stores a set of test program codes scanned-in prior to

ABIST test." (Col. 4, ll. 31-33.) "These 9 bits are divided into 5 fields: three bit Pointer field 14, one bit Address Increment field 15, three bit Data Control field 16, one bit [Read/]Write Control field 17, and one bit End-Of-Address-Space control field 18." (*Id.* ll. 33-37.)

In the Examiner's aforementioned example, we agree with him that because Lo's Array Address Pointer field 14 contains "010," the ABIST would perform the aforementioned steps "repeatedly . . . until the address space has been fully explored. . . ." (Answer 13.) Because the Read/Write Control field 17 contains a "1" in the Examiner's example, however, the exploration would be limited to writing. (Lo, col. 11, ll. 36-37.) Without being able to read, in addition to write, the sequence of procedures specified by the Examiner's "010100011" instruction cannot perform a test. At best, the instruction would only enable preparing for a test. We agree with the Appellants that "[s]ubsequently, a second 9-bit word will be needed with read/write control field 17 set to '0', i.e., in the 'Read mode' so that the array under test can be read to see whether the information which was previously set in under the 'write mode' is correct." (Reply Br. 3.)

The absence of a single instruction specifying a sequence of testing procedures negates anticipation. Therefore, we reverse the anticipation rejection of claims 1 and 18 and of claims 2-9, 13, 16, 17, 19-26, 30, 33, and 34, which depend therefrom.

"In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness." *In re*

Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993)
(citing *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed.
Cir. 1992)). "'A *prima facie* case of obviousness is established when the
teachings from the prior art itself would appear to have suggested the
claimed subject matter to a person of ordinary skill in the art.'" *In re Bell*,
991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting *In re
Rinehart*, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

Here, the Examiner does not allege, let alone show, that the addition
of Gold or Correale cures the aforementioned deficiency of Lo. Therefore,
we reverse the obviousness rejections of claims 10-12, 14, 15, 27-29, 31, and
32, which depend from claims 1 or 18.

VI. CONCLUSION

In summary, the rejection of claims 1-9, 13, 16-26, 30, 33, and 34
under § 102(b) is reversed. The rejections of claims 10-12, 14, 15, 27-29,
31, and 32 under § 103(a) are also reversed.

REVERSED

tdl/ce

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